

REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 1-8, 10-15, and 20-25 are pending in the present application. The foregoing amendment amends Claims 1, 8, 20, and 22 and Figure 23; and cancels Claim 9 without prejudice or disclaimer. No new matter is added.

In the outstanding Office Action, Figure 23 was objected to; Claim 22 was rejected under 35 U.S.C. 112, second paragraph as indefinite; Claims 1-4, 6 and 8 were rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 5,378,914 to Ohzu et al. (hereinafter "Ohzu"); Claims 8-11 and 20-23 were rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,621,132 to Onishi et al. (hereinafter "Onishi"); Claims 5 and 7 were rejected under 35 U.S.C. 103(a) as unpatentable over Ohzu in view of Onishi; and Claims 12-15 were allowed.

Applicants thank the Examiner for the indication of allowable subject matter.

Regarding the objection to Figure 23, that figure is amended in view of the Examiner's comments. Accordingly, Applicants respectfully request the objection to Figure 23 be withdrawn.

Regarding the rejection of Claim 22 under 35 U.S.C. 112, second paragraph, the claim is amended to recite "a fourth semiconductor region of a ~~second~~ first conductivity type ~~provide on~~ provided on the ~~fourth semiconductor region~~ semiconductor layer" in view of the Examiner's comments. Accordingly, Applicants respectfully request that the rejection of Claim 22 under 35 U.S.C. 112, second paragraph, be withdrawn.

Addressing now the rejections of Claims 1-8, 10, 11, and 20-25 under 35 U.S.C. 102 and 103 as anticipated by or unpatentable over Ohzu and/or Onishi, summarized above, those rejections are respectfully traversed. More particularly, Applicants sequentially address each

of rejected independent Claims 1, 8, 20, and 22 and their applied references. The remaining rejected claims depend from Claims 1, 8, 20, and 22.

Amended independent Claim 1 now recites:

a first semiconductor region of a second conductivity type provided under the semiconductor base region, a second semiconductor region of a first conductivity type provided under the first semiconductor region, a third semiconductor region of a second conductivity type provided under the second semiconductor region, and a fourth semiconductor region of a second conductivity type on the semiconductor base region,
the first main electrode being provided on the fourth semiconductor region and the second main electrode being provided under the third semiconductor region.

Applicants' Figure 1 illustrates a non-limiting example of the claimed semiconductor base region (base region 5), first semiconductor region (n-type region 9), second semiconductor region (p-type region 10), third semiconductor region (epitaxial layer 6), and fourth semiconductor region (n-type source region 2). Applicants' Figure 14 illustrates a non-limiting example of the claimed first main electrode (emitter electrode E) and second main electrode (collector electrode C). The above-noted features are neither taught nor suggested by Ohzu.

Amended independent Claim 8 now recites "wherein the second and the third semiconductor regions are substantially depleted, and a boundary between the second semiconductor region and the third semiconductor region is in contact with a side surface of the trench." Applicants' Figure 1 illustrates a non-limiting example of the claimed second semiconductor region (p-type region 10), third semiconductor region (n-type region 9), and trench (trench gate). Applicants' Figure 14 illustrates a non-limiting example of the first main electrode (emitter electrode E) and the second main electrode (collector electrode C). The first and second main electrodes are neither taught nor suggested by Ohzu. The claimed configuration of the second semiconductor region, third semiconductor region, and trench is neither taught nor suggested by Onishi.

Each of amended independent Claims 20 and 22 now recites "the trench [is/being] in contact with the second semiconductor region and the third semiconductor region."


Applicants' Figure 18 illustrates a non-limiting example of the claimed second semiconductor region (p-type region 10), third semiconductor region (n-type region 9), and trench (trench gate). The claimed configuration of the second semiconductor region, third semiconductor region, and trench are neither taught nor suggested by Onishi.

Accordingly, as the above-noted features distinguish independent Claims 1, 8, 20, and 22 over their applied references, Applicants respectfully request that the rejections of Claims 1-8, 10, 11, and 20-25 under 35 U.S.C. 102 and 103 as anticipated or unpatentable over Ohzu and/or Onishi, summarized above, be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 23. This sheet, which includes Fig. 23, replaces the original sheet including Fig. 23.

Attachment: Replacement Sheet